We claim:

1. A vertically structured power semiconductor component, comprising:

a semiconductor body of a first conductivity type and having a first main surface and a second main surface opposite said first main surface;

a body zone of a second conductivity type opposite of said first conductivity type introduced into said first main surface;

a zone of said first conductivity type disposed in said body zone;

a first electrode making contact with said zone and with said body zone;

a second electrode disposed on said second main surface;

an insulating layer disposed on said first main surface;

a gate electrode disposed above said body zone and separated from said body zone by said insulating layer; and

an intersection of said semiconductor body and said body zone defining a pn junction, said semiconductor body having a layer thickness between said pn junction and said second main surface selected such that, when one of a maximum allowed blocking voltage and a voltage just less than this, is applied between said first electrode and said second electrode, a space charge zone created in said semiconductor body meets said second main surface before a field strength created by an applied blocking voltage reaches a critical value.

2. The vertically structured power semiconductor component according to claim 1, wherein said layer thickness of said semiconductor body has a specific charge density ρ in a direction z between said pn junction and said second main surface such that:

$$\int_0^W \rho(z)dz \leq 0.9q_c$$

in which W denotes the layer thickness, and q_c denotes a critical charge quantity in said semiconductor body and is linked to an electric field applied between said first electrode and said second electrode by Maxwell equation:

$$\vec{\nabla}.\vec{E} = -4\pi\rho \ .$$

3. The vertically structured power semiconductor component according to claim 1, wherein said semiconductor body has heavily doped terminal regions of said first conductivity type disposed at said second main surface.

4. The vertically structured power semiconductor component according to claim 3, including a further zone of said first conductivity type disposed in a vicinity of said second main surface.

5. The vertically structured power semiconductor component according to claim 3, wherein said semiconductor body has punch-through regions disposed between said heavily doped terminal regions, and a current/voltage characteristic in breakdown can be controlled through an area ratio between said heavily doped terminal regions and said punch-through regions.

6. The vertically structured power semiconductor component according to claim 1, wherein said semiconductor body has an edge termination and including a channel stopper disposed in an area of said edge termination.

7. The vertically structured power semiconductor component according to claim 6, including a source magnetoresistor disposed above said first main surface.

8. The vertically structured power semiconductor component according to claim 1, including a compensation region of said second conductivity type disposed below said body zone in said semiconductor body.

9. The vertically structured power semiconductor component according to claim 8, wherein said compensation region of said second conductivity type is produced by a plurality of epitaxy and implantation operations.

10. The vertically structured power semiconductor component according to claim 9, wherein said compensation region of said second conductivity type is produced horizontally between said first main surface and said second main surface through same implantation openings.

11. The vertically structured power semiconductor component according to claim 1, wherein said semiconductor body has an edge region and including vertical compensation areas of said second conductivity type disposed in said edge region.